SEMICONDUCTOR DEVICE WIRING AND METHOD OF MANUFACTURING THE SAME

Abstract of the Disclosure

A wiring of a semiconductor device and a method of manufacturing the same are disclosed. A first conductive layer is formed on a semiconductor substrate followed by a first insulation material which is deposited on the first conductive layer to form a first insulation layer. Then, a CMP process is implemented to form the first insulation layer. A second insulation layer is formed by depositing a second insulation material on the first insulation layer in order to cover a scratch formed on the first insulation layer after implementing the CMP process. A first etching pattern is formed by etching the second insulation layer to a thickness less than a thickness of the second insulation layer. Thereafter, a conductive material is deposited on the etching pattern and then a planarizing process is implemented to form a conductive pattern having a damascene shape. The formation of a bridge between neighboring conductive patterns caused by a scratch generated during implementation of CMP process can be prevented to markedly decrease defects in semiconductor devices.

K:\Samsung\134\134patapp2.wpd